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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/768,556	01/25/2001	Yukihiro Inoue	L8462.01101	5136

7590 03/03/2004

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EXAMINER	
GEBREMARIAM, SAMUEL A	
ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 03/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/768,556	INOUE, YUKIHIRO	
	Examiner	Art Unit	
	Samuel A Gebremariam	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/17/03*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5-8 and 11-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-8 and 11-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 14 and 6, are rejected under 35 U.S.C. 103(a) as being unpatentable over Pfiester in view of admitted prior art (figs. 3A-3D).

Pfiester teaches (fig. 3) a semiconductor device comprising: a source side offset diffusion layer region (44) and a drain side offset: diffusion layer region (42) of a second conductivity type in a transistor formed, so as to be separated from each other, in a predetermined region in a region of a first conductivity type in a semiconductor substrate (36); a gate insulator film (48) region formed between the source side offset diffusion layer region (44) and the drain side offset diffusion layer region (42); a gate electrode (46) formed on the gate insulator film region, and a diffusion layer (40) of the first conductivity type of which the impurity concentration is higher than that of the region of the first conductivity type and which is formed so as to surround the source side offset diffusion layer region (44), the drain side offset diffusion layer region (42) and the gate insulator film region, wherein both ends of the gate insulator film region, in a direction substantially perpendicular to a direction from the source offset diffusion layer region to the drain offset diffusion layer region, form protruding portions (54) that, and

wherein the diffusion layer of the first conductivity type is formed so as to surround the protruding portions and so as to be separated from the protruding portions by a predetermined distance.

Pfiester does not explicitly teach that the gate insulator film at the protruding portion makes direct contact with the gate electrode. Pfiester does not show the channel width direction.

Admitted prior art teaches (fig. 3c) that the gate insulator film (9) at the protruding portion (10) makes direct contact with gate electrode.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the protruding portion make direct contact with the gate electrode in the structure of Pfiester as claimed in order to increase breakdown voltage.

Regarding claim 6, Pfiester teaches (fig. 3) the entire claimed structure of claim 14 above including the diffusion layer (40) of the first conductivity type is a channel stopper region.

3. Claims 13 and 5, are rejected under 35 U.S.C. 103(a) as being unpatentable over Pfiester, admitted prior art and in view of Nagatomo et al. US Patent No. 5,164,806.

Regarding claim 13, Pfiester teaches substantially the entire claimed structure of claim 14 above including a position of an end of the diffusion layer of the first conductivity type at each parts surrounding the protruding portions substantially coincides with a position of an end of each of the protruding portions.

Pfiester does not teach the diffusion layer is formed so as to be in contact with the protruding portions.

Nagatomo teaches (fig. 4) forming region (15) between region (5a) and channel stop layer (8) for forming MOS transistor. The formation of region (15) increases the breakdown voltage of the junction.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the impurity region taught by Nagatomo in the structure of Pfiester in order to increase breakdown voltage. The modified structure of Pfiester would have the diffusion layer contacting the protruding portion.

Regarding claim 5, Pfiester teaches substantially (fig. 3) the entire claimed structure of claim 13 above including the diffusion layer (40) of the first conductivity type is a channel stopper region.

4. Claims 11, 12, 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pfiester, admitted prior art, Nagatomo in view of Murakami US patent No. 4,819,045.

Regarding claims 11 and 12, Pfiester teaches substantially (fig. 3) the entire claimed structure of claims 13 and 14 above including the source side offset diffusion layer and the drain side offset diffusion layer are lower in impurity concentration than diffusion layer.

Pfiester fails to teach the transistor is a high voltage transistor.

The use of MOS transistors for high voltage application is conventional and also Murakami teaches the use MOS transistor for high voltage application.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the structure of Pfiester for high voltage application as taught by Murakami for improved withstand of high voltage application.

Regarding claims 7 and 8, Pfiester teaches substantially (fig. 3) the entire claimed structure of claims 13 and 14 above including the diffusion layer of the first conductivity type is a channel stopper region (40).

Response to Arguments

4. Applicant's arguments with respect to claims 5-8 and 11-14 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel Admassu Gebremariam whose telephone number is 703 305 1913. The examiner can normally be reached on 8:00am-4: 30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571)) 272-1732. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Samuel Admassu Gebremariam
February 23, 2004

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800